Design and Development of Advanced Low Power Hybrid Acquisition (ALPHA) ASIC for Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope (ADAPT)

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***Abstract*—We present the design and development of low power operation ASIC called ALPHA. ALPHA operates at 256MHz, and it is capable of 100 mega samples per second (MSa/s) waveform sampling with 16 input channels. Multiple ALPHAs operate in a daisy chain format, and they are connected to a single FPGA. The ALPHA was manufactured by TSMC, and the functionality of the digital block was tested. This paper discusses the preliminary results of the evaluation.**

***Index Terms*—ALPHA, FPGA, CT5TEA, daisy chain, sampling, ADC, readout**

I. Introduction

This paper discusses the design and development of an Application Specific Integrated Circuit (ASIC) named ALPHA for the Advanced Particle-astrophysics Telescope (APT) sensor elements readout. ALPHA is responsible for scintillating fiber-trackers, and imaging calorimeters to measure gamma-rays and other cosmic-rays. The readout process includes analog sampling, sample conversion with an Analog to Digital Converter (ADC), output-data packet transmission, and collection to Field Programmable Gate Arrays (FPGA).

II. Design and Architecture

Novel in this architecture is the daisy-chaining of the readout, as well as sharing of clocking resources, all to reduce power. For the readout sequence and the data transmission sequence to work adequately, two data paths, two token paths, and two sampling banks are featured. Two paths can bypass any defective ALPHAs, and a token is used for collision avoidance in the data transmission path. The token and data packet transmit in opposite direction from each other. A token starts from the FPGA initially and loops around the daisy chain until the ADAPT ends its mission. On the other hand, the data packets start from each ALPHA. When a token reaches an ALPHA that has a data packet that is waiting to shift out, the data packet starts shifting through the data path toward the FPGA for collection.

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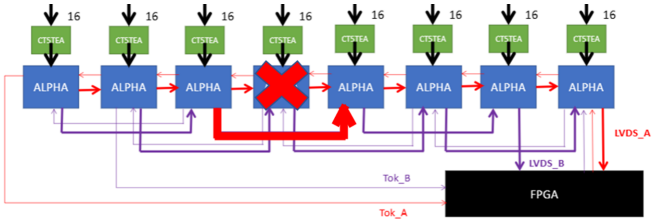

Fig. 1. Demonstrate single-pointASIC fault tolerance.

A. Sampling mechanism for ALPHA

The first research challenge is the data collection method. ALPHA has two sampling banks to reduce the sampling dead time. Active bank of either A or B of all 16 channels are always sampling and await a trigger from CT5TEA.

When a trigger happens, certain interval before the trigger ; this is called Look back window (LBW), and another certain interval after the trigger ; this is called sample after trigger (SAT), the samples in these intervals will be captured.

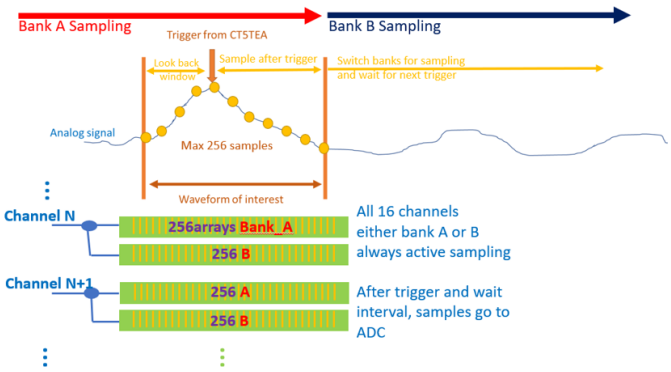

Fig. 2. Sampling mechanism.

B. Analog Sample Banks plus ADC

The analog samples are stored in a capacitor array and proceed to the conversion state directly without being stored in registers. While one bank is busy in the conversion state, the other bank is already sampling. This is how it reduces sampling dead time.

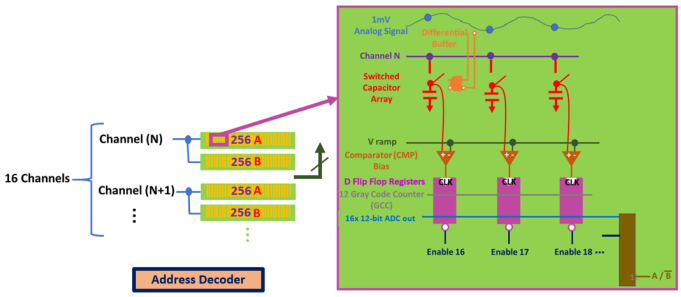

Fig. 3. Analog Sample Banks plus ADC.

C. Output data packet

After the analog to digital conversion is done, an output packet is created. Figure 4 shows the format of an output packet. Header section starts with a start word ALPHA. In the middle section, all the digitized data with the channel information. The footer section ends with the trailer word OMEGA.

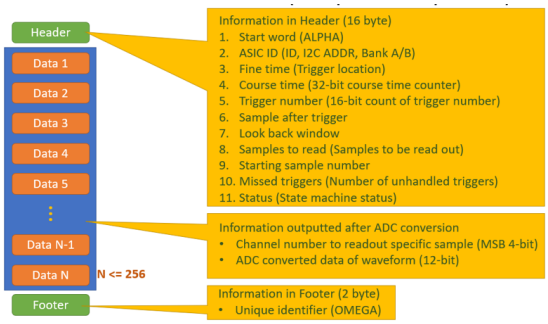

Fig. 4. Output data packet.

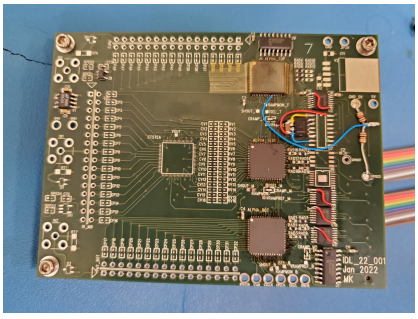

Fig. 5. ALPHA Evaluation PCB.

III. Results

A. Global reset working

When a global register reset is issued initially, we observe a token output from ALPHA.

B. Token passing working

When a token is sent to ALPHA, we observe it comes back out to FPGA.

C. Trigger receiving and data shift out success

After a trigger is issued, we see the data output stream after some interval for ADC process.

D. Output data expected to be header and footer observed

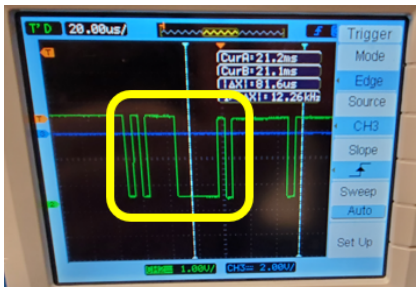

Fig. 6. Header ALPHA (xA1FA).

E. De-Serialization of the output data packet success

The serialized output data packet was de-serialized. We can see ALPHA as a header of the stream, and we observe OMEGA as a footer word.

F. Successful in observing ramp signal

We are able to observe the ramp signal. By varying the ISEL value, the ramp rise time differs, and the plot shows results.

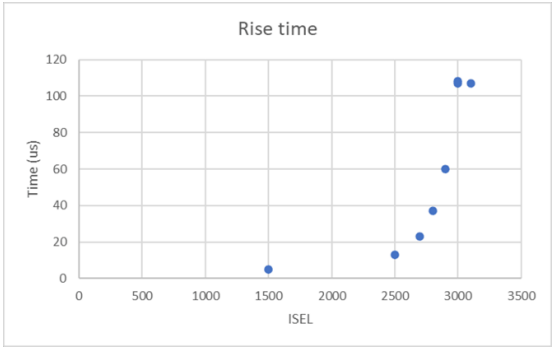

Fig. 7. ISEL vs Rise Time.

G. Two types of Test Mode setting is working

IV. Conclusion

In conclusion, the digital block of ALPHA functions as expected. During my presentation, the design, applications, testing and functionality will be discussed.